IN THE CLAIMS:

Please delete the paragraph heading on page 24 of the English translation of the subject application, line 1, and insert in place thereof the paragraph heading as follows:

--CLAIMS--

Please delete the paragraph heading on page 24 of the English translation of the subject application, line 3, and insert in place thereof the paragraph heading as follows:

-- What is claimed is: --.

Please amend the claims as follows:

1. (Currently Amended) Viterbi decoder for decoding a received sequence of data symbols which are coded using a predetermined coding instruction, and are transmitted via a transmission channel, having:

(a) a branch metric calculation circuit (~~5~~) for calculation of branch metrics (~~λ~~) for the received sequence of coded data symbols;

(b) a path metric calculation circuit (~~9~~) for calculation of path metrics (~~γ~~) and decision values (~~δ_s~~) as a function of the branch metrics (~~λ~~) and the coding instruction, with the calculated path metrics (~~γ~~) in each case being compared with an adjustable decision threshold value (~~SW~~) in order to produce an associated logic validity value (~~VALID~~), in which case the decision threshold value (~~SW~~) for the path metric normalization can be set such that it is variable;

(c) a selection circuit (~~20~~) which temporarily stores only those path metrics (~~γ~~) whose validity value (~~VALID~~) is logic high in a memory, and selects from the temporarily stored path metrics (~~γ~~) that path with the optimum path metric, with an increasing number of decision values (~~δ_s~~) being stored in the selection circuit (~~20~~) as the signal-to-noise ratio (~~SNR~~) of the transmission channel decreases.

2. (Currently Amended) Viterbi decoder according to Claim 1, ~~characterized in that~~ wherein the selection circuit (~~20~~) emits the data symbol sequence which is associated with the selected path for further data processing.

3. (Currently Amended) Viterbi decoder according to Claim 1 ~~or 2, characterized in that~~, wherein the path metric calculation circuit (~~9~~) sets the validity

value ~~(VALID)~~ of logic high when the associated calculated path metric is less than the threshold value ~~(SW)~~.

4. (Currently Amended) Viterbi decoder according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the selection circuit ~~(20)~~ selects the path with the lowest calculated path metric.

5. (Currently Amended) Viterbi decoder according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the path metric calculation circuit ~~(9)~~ contains two or more path metric calculation elements ~~(10)~~.

6. (Currently Amended) Viterbi decoder according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein a path metric calculation element ~~(10)~~ in each case calculates the path metrics of two paths and compares them with one another, and emits the lower of the two path metrics to an associated clock memory element ~~(18)~~ for temporary storage.

7. (Currently Amended) Viterbi decoder according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the path metric calculation element ~~(10)~~ has:

(a) a first adder ~~(26)~~, which adds the branch metric of a first path and the metric of the first path which is temporarily stored in the associated clock memory element ~~(18)~~, and emits this to a first input ~~(31)~~ of a multiplexer ~~(32)~~,

(b) a second adder ~~(27)~~, which adds the branch metric of a second path and the path metric of the second path which is temporarily stored in the associated clock memory element ~~(18)~~, and emits this to a second input ~~(39)~~ of the multiplexer ~~(32)~~,

(c) a first comparator circuit ~~(35)~~, which compares the sum values calculated by the two adders ~~(26, 27)~~, with the comparison result being emitted as a decision value ~~(δ_s)~~ to the selection circuit ~~(20)~~ and to the multiplexer ~~(32)~~ as a control signal, with the multiplexer ~~(32)~~ passing on the lower of the sum values calculated by the two adders ~~(26, 27)~~ to the associated clock register ~~(18)~~;

(d) a second comparator circuit ~~(50)~~, which compares the passed-on sum value with the adjustable decision threshold value ~~(SW)~~ and emits a logic high validity value ~~(VALID)~~ when the passed-on sum value is less than the decision threshold value ~~(SW)~~.

8. (Currently Amended) Viterbi decoder according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the adjustable decision threshold value ~~(SW)~~ is a power value to the base two.

9. (Currently Amended) Viterbi decoder according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein two or more logic validity values which are produced by the path metric calculation circuit ~~(9)~~ are logically OR-linked by a logic circuit, and all the associated decision values are temporarily stored in the memory of the selection circuit ~~(20)~~ when the result of the logical OR linking is logic high.

10. (Currently Amended) Viterbi decoder according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the path metrics are calculated sequentially by the path metric calculation elements ~~(10)~~.

11. (Currently Amended) Viterbi decoder according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein a number of path metrics, which correspond to the number N_{TS} of states in a trellis diagram, are calculated using 2^K path metric calculation elements, and in that the number 2^K of calculation element is given by:

$$1 \leq 2^K \leq \frac{N_{TS}}{2} .$$

12. (Currently Amended) Viterbi decoder according to Claim 11, ~~characterized in that~~ wherein the path metric calculation elements ~~(10a–10i)~~ are butterfly calculation elements, and in that the number 2^K of calculation element is given by:

$$1 \leq 2^K \leq \frac{N_{TS}}{2} .$$

13. (Currently Amended) Viterbi decoder according to Claim 12, ~~characterized in that~~ wherein the path metric calculation elements ~~(10a-10c)~~ are add-compare calculation elements, and in that the number 2^K of calculation element is given by:

$$1 \leq 2^K \leq N_{TS}.$$

14. (Currently Amended) Viterbi decoder according to ~~one of the preceding claims, characterized in that~~ claim 1, wherein the coding instruction is a trellis code, which has 2^L state transitions, where

$$0 \leq L < \infty$$

and L is a natural number.

15. (Currently Amended) Viterbi decoder according to Claim 11, ~~characterized in that~~ wherein the trellis code has two state transitions.

16. (Currently Amended) Method for decoding a coded sequence of data symbols which are coded using a predetermined coding instruction, having the following steps:

(a) reception of the coded data symbol sequence via a transmission channel;

(b) calculation of branch metrics ~~(λ)~~ for the received data symbol sequence;

(c) calculation of path metrics ~~(γ)~~ and decision values ~~(δ_s)~~ for the received data symbol sequence as a function of the branch metrics ~~(λ)~~ and the coding instruction;

(d) comparison of the calculated path metrics ~~(γ)~~ with a decision threshold value ~~(SW)~~ for production of logic validity values ~~(VALID)~~, in which case the decision threshold value ~~(SW)~~ for path metric normalization can be set such that it is variable;

(e) storage of those calculated path metrics ~~(γ)~~ whose validity values ~~(VALID)~~ are logic high in a temporary store, with an increasing number of decision values ~~(δ_s)~~ being stored as the signal-to-noise ratio ~~(SNR)~~ of the transmission channel decreases;

(f) selection of that path whose stored path metric is a minimum;

(g) determination of the data symbol sequence associated with the selective path, by means of the coding instruction;

(h) emission of the determined data symbol sequence for further data processing.